REMARKS

Addressing Claim Rejections – 35 USC section 102

[1] The Examiner rejected claims 1-3, 6-17, 22-26 and 36-38 as anticipated by Tour – Pub No. US 2003/0058697. Applicant respectfully disagrees that Tour anticipates any of the claims in the LINCOLN invention.

[2] Regarding claims 1, 2, 3 and 16. Examiner substantially describes, inter alia, Tour's teaching in paragraph 48 that the process is iterative and the steps repeated until programming is complete. Referring to Tour's Fig 1, the iterative nature of the Tour approach is further illustrated. By contrast, Applicant is teaching and claiming programming using *contiguous sets* of external connections. Tour does not include a teaching of contiguous sets as taught by Applicant.

[3] With respect to claim 17, Tour illustrates, as set forth in paragraph 48 and in the remaining text and figures cited by the Examiner, the use of a single pulse. Notable is the articulation that Tour provides for limited switching. Nowhere in paragraph 48 of Tour or in any other text or diagram is programming taught where more than a single device is programmed via external connections. Applicant believes Tour does not anticipate claim 17 and respectfully suggests claim 17 be allowed as amended. The remainder of the Examiner's rejections (claims 22-26, and 36-38) are overcome because the underlying independent claim is not anticipated by Tour.

[4] Applicant respectfully submits that the 102(e) rejection of claims 1-3,6-17, 22-26 and 36-38 is overcome; Applicant's claims 1-3, 6-17, 22-26 and 36-38 are in condition for allowance and Applicant requests the Examiner to allow the claims.

Addressing Claim Rejections – 35 USC section 103

[5] The Examiner has applied 35 USC section 103 in rejecting claims 4 and 5. In light of the non-anticipation of Tour, as set forth above, the combination of Tour and Jain cannot render the Applicant's invention obvious. Applicant submits that claim 4 and 5 are in condition for allowance and requests the Examiner to allow claim 4 and 5..

Allowable Subject Matter

[6] The Examiner has indicated that claims 18-21 are allowable if rewritten in independent form to overcome dependence on claim 17. Applicant respectfully submits that the 102(e) rejection of claim 17 has been overcome for the reasons set forth hereinabove. Because claim 17 is in condition for allowance as amended, claims 18-21 need not be amended and are allowable as originally written. Applicant respectfully requests the Examiner to allow claims 18-21 as written.

[7] Examiner has allowed claims 27-35 and claims 39-43. Applicant respectfully submits the remaining claims, 1-26, 36-39 are in condition for allowance and requests Examiner so allow.

[8] If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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APPENDIX

CLAIM VERSION MARKED WITH CHANGES MADE TO CLAIMS

1. (original) A method for discovering a connectivity relationship among a plurality of external connections to a two dimensional logic cell, the method comprising the steps of:

(e) for all contiguous sets of one or more of the external connections, applying a voltage to each contiguous set and measuring a total current flow received by the remainder of the external connections;

(f) examining a current flow measurement corresponding to a contiguous set of the external connections;

(g) grouping the contiguous set of external connections if the measured current flow falls below a threshold; and

(h) repeating steps (b)-(c) for different contiguous sets of external connections.

2. (original) The method of claim 1 wherein each previously grouped set of external connections is treated as a single external connection.

3. (original) The method of claim 1 further comprising the step of using the connection groupings to discover a logical relationship among the external connections.

4. (original) The method of claim 3 wherein the connection groupings are used to generate an ordered binary decision diagram (OBDD).

5. (original) The method of claim 4 wherein the connection groupings comprise a set of variables and orderings on those variables that are used to generate the OBDD.

6. (original) The method of claim 1 wherein the current flow threshold is predetermined.

7. (original) The method of claim 1 wherein the current flow threshold is dynamically determined.

8. (original) The method of claim 1 wherein the logic cell is a nanocell.

9. (original) The method of claim 8 wherein the nanocell is a regular polygon.

10. (original) The method of claim 9 wherein the regular polygonal nanocell is further characterized by one or more external connections on one or more sides of the polygon.

11.(original) The method of claim 9 wherein each side of the polygonal nanocell has at least one external connection.

12. (original) The method of claim 9 wherein the nanocell has at least 20 external connections.

13. (original) The method of claim 9 wherein the nanocell has at least 4 external connections.

14. (original) The method of claim 9 wherein the nanocell includes an assembly of nanocells which are of one or more planar geometries.

15. (original) The method of claim 14 wherein discovery of connectivity relationships is at least partially effected by or through neighboring nanocells.

16. (original) A method for discovering a connectivity relationship among a plurality of external connections to a two dimensional logic cell, the method comprising the steps of:

(e) applying a voltage to a contiguous set of one or more of the external connections;

(f) measuring a total current flow received by the remainder of the external connections;

(g) grouping the contiguous set of external connections if the measured current flow falls below a threshold; and

(h) repeating steps (a) – (c) for different contiguous sets of external connections.

17. (currently amended) A method for programming a series of interconnected devices, wherein each device is capable of assuming at least two stable states, the devices initially being in a first state, the method comprising the step of:

applying a voltage pulse to an input to the devices, the voltage pulse having a first polarity and a time duration sufficient to cause a number x (where x is greater than 1) of devices to switch to a second state.

18. (original) The method of claim 17 further comprising the step of applying a second voltage pulse to the input, the second pulse having a second polarity and a duration sufficient to cause a number y of devices to return to the first state, where y is less than x.

19. (original) The method of claim 18 further comprising the step of applying subsequent voltage pulses to the input, the subsequent voltage pulses having alternating polarity and progressively shorter duration.

20. (original) The method of claim 19 wherein the numbers x and y are predetermined.

21. (original) The method of claim 19 wherein the numbers x and y are dynamically determined.

22. (original) The method of claim 17 wherein the interconnected devices are molecular switches having a characteristic negative differential resistance.

23. (original) The method of claim 17 wherein the logic cell includes switching devices of different switching potentials.

24. (original) The method of claim 17 further including the step of devices assuming a known state at some time subsequent to the application of the first pulse.

25. (currently amended) The method of claim 17 wherein the interconnected devices are molecular switches within nanocells, and wherein logic cell programming is at least partially effected by or through neighboring nanocells.

26. (original) A method for re-programming a series of interconnected devices, wherein each device is capable of assuming at least two stable states, the devices initially being in an operational state, the method comprising the step of:

applying a voltage pulse to an input to the devices, the voltage pulse having a first polarity and a time duration sufficient to cause a number x of devices to switch to a second state.

27. (original) A method for programming a logic cell having a plurality of external connections interconnected by a plurality of switching devices, the method comprising the steps of:

(e) discovering a logical relationship among the external connections to the logic cell;

(f) programming the switchable devices to perform a logic function by using a series of voltage pulses having alternating polarity and progressively shorter duration;

(g) testing the logic cell to determine if it performs the programmed logic function;

(h) repeating steps (a)-(c) as necessary to ensure the logic cell performs the programmed logic function.

28. (currently amended) A method for programming a logic cell having a plurality of external connections interconnected by a plurality of switching devices, the method comprising the steps of:

(c) discovering a logical relationship among the external connections to the logic cell;

(d) programming the switchable devices to perform a logic function by using a series of voltage pulses having alternating polarity and progressively shorter duration, where the sequence of duration, voltages and choice of inputs on which to signal those sequences of voltages is chosen based on a logical representation of connectivity within the logic cell;

(c) testing the logic cell to determine if it performs the programmed logic function.

29. (currently amended) The method of claim 28 wherein the logic cell comprises one or more nanocells[[,]].

30. (currently amended) A method of re-programming, modifying or repairing a logic cell having a plurality of external connections interconnected by a plurality of switching devices, the method comprising the steps of:

(d) determining the operable function of the logic cell;

(e) re-programming the switchable devices to perform a selected logic function by using a series of voltage pulses having alternating polarity and progressively shorter duration; and

(f) confirming operability of the programmed logic cell.

31. (original) The method of claim 30 further characterized by performance of the steps after and during such time as the logic cell has commenced an operational mode.

32. (original) The method of claim 30 wherein the voltage pulses are selected so as to preferentially influence a subset of the switching device types according to the threshold potential of that subset.

33. (currently amended) A method of re-programming, modifying or repairing a logic cell, including the case where such logic cell is a nanocell, such logic cell having a plurality of external connections interconnected by a plurality of switching devices, the method comprising the steps of:

(d) determining the operable function of the logic cell;

(e) re-programming the switchable devices to perform a selected logic function by using a series of voltage pulses having alternating polarity and progressively shorter duration, and where the sequence of duration, voltages and choice of inputs on which to signal those sequences of voltages is chosen based on a logical representation of connectivity within the logic cell; and

(f) confirming operability of the programmed logic cell.

34. (original) The method of claim 33 further characterized by performance of the steps after and during such time as the logic cell has commenced an operational mode.

35. (original) The method of claim 33 wherein the voltage pulses are selected so as to preferentially influence a subset of the switching device types according to the threshold potential of that subset.

36. (currently amended) A device containing at least one logic cell programmed by the method of claim 1.

37. (original) A device containing at least one logic cell programmed by the method of claim 17.

38. (original) A device containing at least one logic cell programmed by the method of claim 26.

39. (original) A device containing at least one logic cell programmed by the method of claim 27.

40. (original) A device containing at least one logic cell programmed by the method of claim 28.

41. (original) A device containing at least one logic cell programmed by the method of claim 29

42. (original) A device containing at least one logic cell programmed by the method of claim 30.

43. (original) A device containing at least one logic cell programmed by the method of claim 33.